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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/679,544	10/06/2000	George Yen	BHT/3092/149	8529

7590 08/17/2004

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EXAMINER	
VO, TIM T	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 08/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/679,544	YEN, GEORGE	
	Examiner	Art Unit	
	Tim T. Vo	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-16,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-16,19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Part III DETAILED ACTION

Notice to Applicant(s)

This application has been examined. Claims 12-16 and 19-20 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 12-16 and 19-20 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kobayashi patent number 6,199,122 refer hereinafter (Kobayashi) in view of Estakhri et al. patent number 6,182,162 refer hereinafter (Estakhri).

As for claims 12 and 20, Kobayashi teaches a disk module of solid state, comprising:

an interface (see figures 1, 12, element 121), being a connector to engage with the main board of a computer (see figures 1, 12, wherein the interface is connected to the board of the computer);

a flash memory controller electrically connected to the connector interface (see figures 1, 12, element 124 ATA controller, connector 123), being used to control data access and specify an address of data storage (see figure 1, ATA controller controls data access and specify address of flash memory 13);

a power source having power input terminal and a power output terminal and connected to the flash memory controller supply a working voltage (see figure 1, wherein the ATA controller receives power supplied from the computer system via interface USB 121 and the output power to the connector 125);

a flash memory array having a plurality of flash memories (see figures 1, 12, flash memory array 13), the flash memory array being connected to the flash memory controller for saving data (see figure 1, 12, flash memory array 13 is connecting to the ATA controller 124), the flash memory controller and the flash memory array are electrical connected to a circuit board (see figures 1, 12, wherein the ATA controller 124, flash memory array are connecting to each other and receiving power from the computer system), the flash memory controller and the flash memory array are enclosed by a casing (see figure 1, 12, wherein the ATA controller 124 and Flash memory 13 are connecting to each other thus connecting to the interface 111 of the computer system);

Kobayashi does not expressly teach IDE interface. However, having an IDE interface in computer system is well known and expected in the art. Estakhri teaches different interface devices in a variety of configurations such as USB bus mode, PCMCIA mode, and ATA IDE mode in the computer system (see abstract of Estakhri). It would have been obvious to include variety interface configurations in the computer of Kobayashi because it would provide compatibility with other interfaces for future system expansion.

As for claims 13-15, Kobayashi teaches flash memory controller is a single chip controller (see figures 1, 12, ATA controller 124).

As for claim 16, Kobayashi teaches wherein plurality of flash memories comprises ten flash memory divided into five group (see figures 1, 12, flash memory array 13).

As for claim 19, Kobayashi teaches the power source extends a power output (see figure 1, power source battery column 4 lines 18-20).

Response to Arguments

2. Applicant's arguments filed 05/10/04 have been fully considered but they are not persuasive.

In response to the applicant's arguments that even Kobayashi and Estakhri were combined as suggested by the examiner, the resultant of the combination does not suggest 1) the flash memory controller and the flash memory array are electrically connected to the circuit board and 2) the flash memory array are enclosed by a casing; 3) nor does the combination suggest a power source having a power input and a power output terminal. In the previous office action, examiner stated that Kobayashi does not expressly teach IDE interface and the examiner combined the teaching of an IDE interface of Estakhri for compatibility with other interfaces for future system expansion. Since Kobayashi teaches the ATA (Advanced Technology Attachment) it means that the computer system of Kobayashi is designed to have attachment ability to the system and therefore the system is ready to accept attach devices to the system for future system expansion. Therefore it would have been obvious to have an IDE interface of Estakhri

to connect the mass storage device memory 13. Further the IDE interface is designed to connect mass storage devices and figure 11 discloses the USB interface 121 is being connect to the circuit board of the computer. 2) Figure 11 discloses the memory card 13 is a flash memory array and it is enclosed within a case as shown in figure 2. 3) Figure 1 discloses the USB interface 121 is connected to the reader/writer 12 and it is known that the computer supplies power to the reader via the USB cable to provide power to utilize the read/write of the attached mass storage device 13.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim T. Vo whose telephone number is 703-308-5862. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

08/16/2004

Tim T. Vo
Primary Examiner
Art Unit 2112